We claim:

1. A process for making an integrated circuit device, comprising:

a. forming a gate insulating layer on a substrate having a first conductivity type and a gate electrode on the gate insulating layer;

b. forming first and second source/drain regions on the substrate adjacent sides of the gate electrode, each source/drain region having a second conductivity type opposite the first conductivity type, the first source/drain region defining the location of a capacitor buried contact; and

c. implanting a second conductivity type dopant into at least a portion of the first source/drain region.

2. A process for making an integrated circuit device according to Claim 1, wherein the second conductivity type dopant is phosphorous.

3. A process for making an integrated circuit device according to Claim 2, wherein the phosphorous is implanted at an energy level of up to 200 KeV.

4. A process for making an integrated circuit device according to Claim 2, wherein the phosphorous is implanted to a depth of up to about 2,000 angstroms.

5. A process for making an integrated circuit device according to Claim 2, wherein the phosphorous is implanted at doses of about 10^{13} ions per square centimeter.

6. A process for making an integrated circuit device, comprising:

a. forming a gate insulating layer on a substrate having a first conductivity type and a gate electrode on the gate insulating layer;

b. implanting a first conductivity type dopant into the substrate on opposite sides of the gate electrode;

c. implanting a second conductivity type dopant into portions of the substrate on opposite sides of the gate electrode previously doped to a first conductivity type in step (b) to form first and second source/drain regions, the first source/drain region defining the location of a buried contact; and

d. implanting a second conductivity type dopant into at least a portion of the first source/drain region.

7. A process for making an integrated circuit device according to Claim 6, wherein the first conductivity type dopant is boron.

8. A process for making an integrated circuit device according to Claim 7, wherein the boron is implanted at an energy level in the range of 25 KeV to 50 KeV.

9. A process for making an integrated circuit device according to Claim 8, wherein the boron is implanted to a depth of approximately 1,000 angstroms.

10. A process for making an integrated circuit device according to Claim 6, wherein the second conductivity type dopant of step (d) is phosphorous.

11. A process for making an integrated circuit device according to Claim 10, wherein the phosphorous is implanted at doses of about 10^{13} ions per square centimeter and an energy level of up to 200 KeV.

12. A process for making an integrated circuit device according to Claim 11, wherein the phosphorous is implanted to a depth of up to about 2,000 angstroms.

13. A process for making an integrated circuit device according to Claim 6, further comprising:

a. forming a first conductor in electrical contact with the first source/drain region;

b. forming a dielectric layer over of the first conductor; and

c. forming a second conductor over the dielectric layer and the first conductor.

14. A process for making an integrated circuit device according to Claim 13, wherein the first conductor is made of polysilicon doped to the second conductivity type.

15. A process for making an integrated circuit device according to Claim 14, wherein the polysilicon first conductor is doped with phosphorous to a level in the range of $1x10^{19}$ to $1x10^{20}$ atoms per cubic centimeter.

16. A process for making an integrated circuit device according to Claim 13, further comprising:

a. forming an upper insulating layer over the structure previously formed;

b. patterning and etching the upper insulating layer and continuing to etch down to expose portions of the second source/drain region; and

c. forming a bit line contact in electrical contact with the exposed portions of the second source/drain region.

17. In a process for forming an integrated circuit device, the device comprising a semiconductor substrate having a first conductivity type, a gate insulating layer on the substrate, a gate electrode on the gate insulating layer, and a source/drain region having a second conductivity type in the surface of the substrate adjacent one side of the gate electrode, the process comprising;

a. implanting a second conductivity type dopant into at least a portion of the source/drain region; and

b. forming a polysilicon conductor in electrical contact with the source/drain region.

18. A process for making an integrated circuit device according to Claim 17, wherein the second conductivity type dopant is phosphorous.

19. A process for making an integrated circuit device according to Claim 18, wherein the phosphorous is implanted at doses of about 10^{13} ions per square centimeter and an energy level of up to 200 KeV.

20. A process for making an integrated circuit device, comprising:

a. forming a gate insulating layer on a substrate having a first conductivity type and a gate electrode on the gate insulating layer;

b. implanting a first conductivity type dopant into the substrate on opposite sides of the gate electrode;

c. implanting a second conductivity type dopant into portions of the substrate on opposite sides of the gate electrode previously doped to a first conductivity type in step (b) to form first and second source/drain regions, the first source/drain region defining the location of a buried contact;

d. forming an insulating layer over the structure previously formed;

e. patterning and etching the insulating layer to form substantially vertical spacers along opposite sides of the gate electrode and to expose a portion of the first source/drain region; and

f. implanting a second conductivity type dopant into the exposed portion of the first source/drain region.

21. A process for making an integrated circuit device according to Claim 20, wherein the spacer etch is self-aligned to a vertical portion of the insulating layer.

22. A process for making an ingegrated circuit device according to Claim 20, further comprising:

a. forming a first conductor in electrical contact with the first source/drain region;

b. forming a dielectric layer over of the first conductor; and

c. forming a second conductor over the dielectric layer and the first conductor.

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